

# 200mA Sink Digital Output Drivers, 24 Channels

Spi interface from Fpga

Convert fpga .8/2V logic to .8V/5.5V logic

Serial output latch, open collector .3A/30V outputs

LVC3.3Vin/Vout, .8/2V, 8mA, no diode  
Spi Interface to/from Fpga

ExtDout B 595 CS  
ExtDout B 595 Selk  
SPI Com Moso Data

CS=Rclk

Selk=Sck

Moso Data=SER\_IN

no Glitch

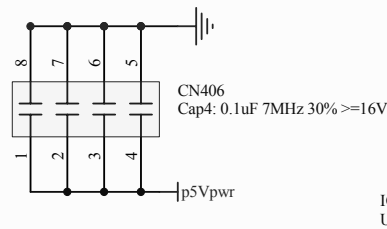
no Glitch

'595 clocks in a din bit

'595 latches data

0.4/4.8V logic

Tpic595 needs 85% \* 4.5V = 3.8V for logic 1



IC: 8x buff, 2Vin 5Vout, Tssop-20, #74AHCT244PWR U455B

Sftwr Rst Hi 5Vpwr

1=SftRst,0=Run, .8/2Vlogic, For 3.3Vpwr IC's

IC: 8x buff, 2Vin 5Vout, Tssop-20, #74AHCT244PWR U455A

Sftwr Rst Lo

LVC3.3Vout, 0=sftwr rst, 1=run

IC: 8x buff, 2Vin 5Vout, Tssop-20, #74AHCT244PWR U455H

IC: 8x buff, 2Vin 5Vout, Tssop-20, #74AHCT244PWR U455E

IC: 8x buff, 2Vin 5Vout, Tssop-20, #74AHCT244PWR U455D

sRstHi 5V

DoutB CS 5V

sRstLo 5V

DoutB Selk 5V

Moso 5V

Low turns on outputs

Move data to output latch, Pos Edge

0=clr register

Selk, Pos Edge, Fpga to '595

Serial Data, Fpga to '595

ExtDoutB [0..15]

OutEN

RCK ↑

SCLR

SCK ↑

SER\_IN

PGND

PGND

PGND

PGND

PGND

PGND

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QA

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QE

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ExtDoutB 0

ExtDoutB 1

ExtDoutB 2

ExtDoutB 3

ExtDoutB 4

ExtDoutB 5

ExtDoutB 6

ExtDoutB 7

serial data out

DoutB SO

ExtDoutB 8

ExtDoutB 9

ExtDoutB 10

ExtDoutB 11

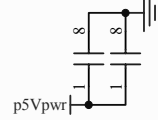
ExtDoutB 12

ExtDoutB 13

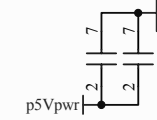
ExtDoutB 14

ExtDoutB 15

Place Caps close to Tpic6a  
CN401A Cap4: 0.1uF 7MHz 30% >=16V  
CN400A Cap4: 0.1uF 7MHz 30% >=16V



Place Caps close to Tpic6a  
CN401B Cap4: 0.1uF 7MHz 30% >=16V  
CN400B Cap4: 0.1uF 7MHz 30% >=16V



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